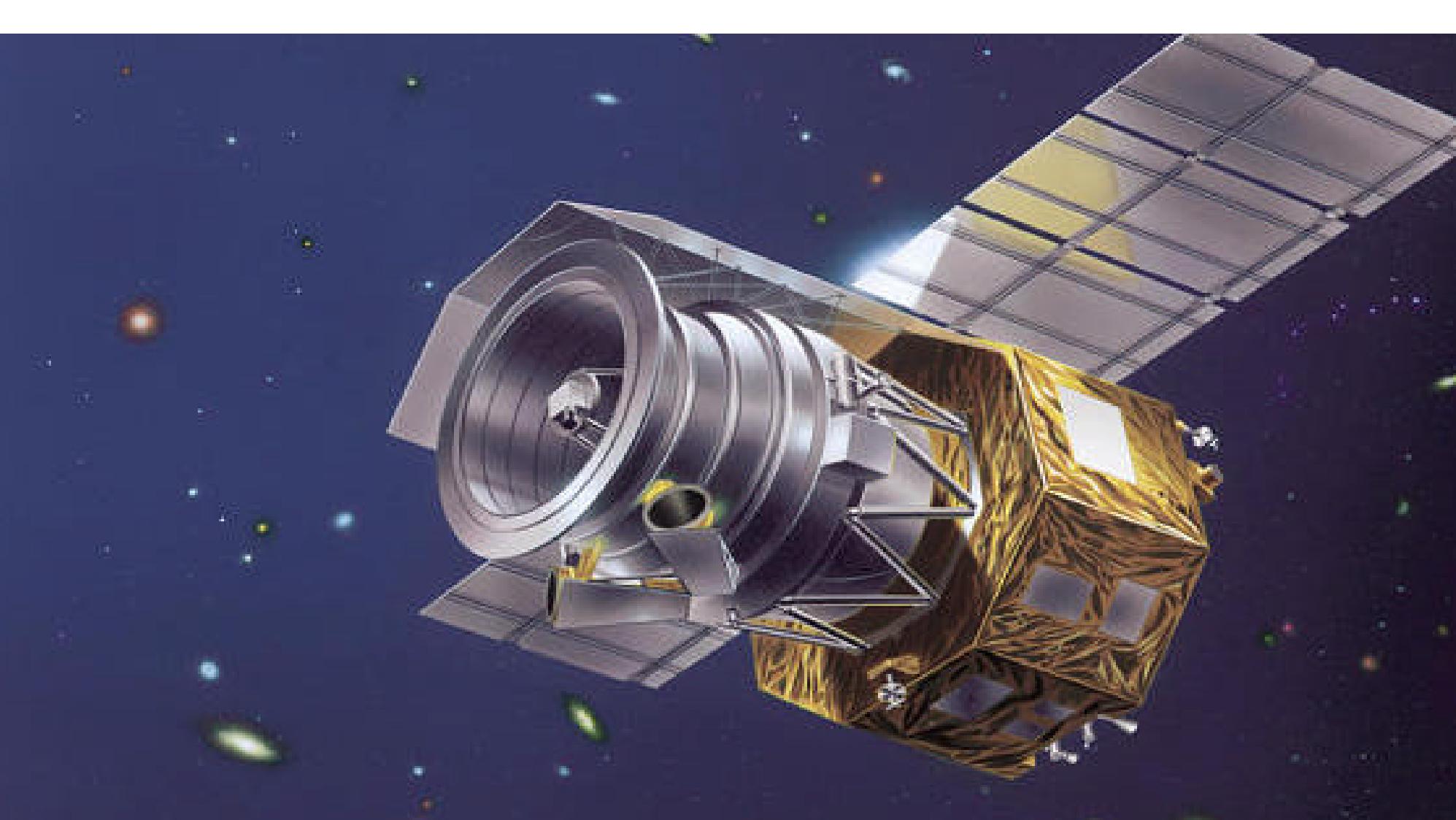


# Evaluation of Cryogenic Readout Electronics for ASTRO-F

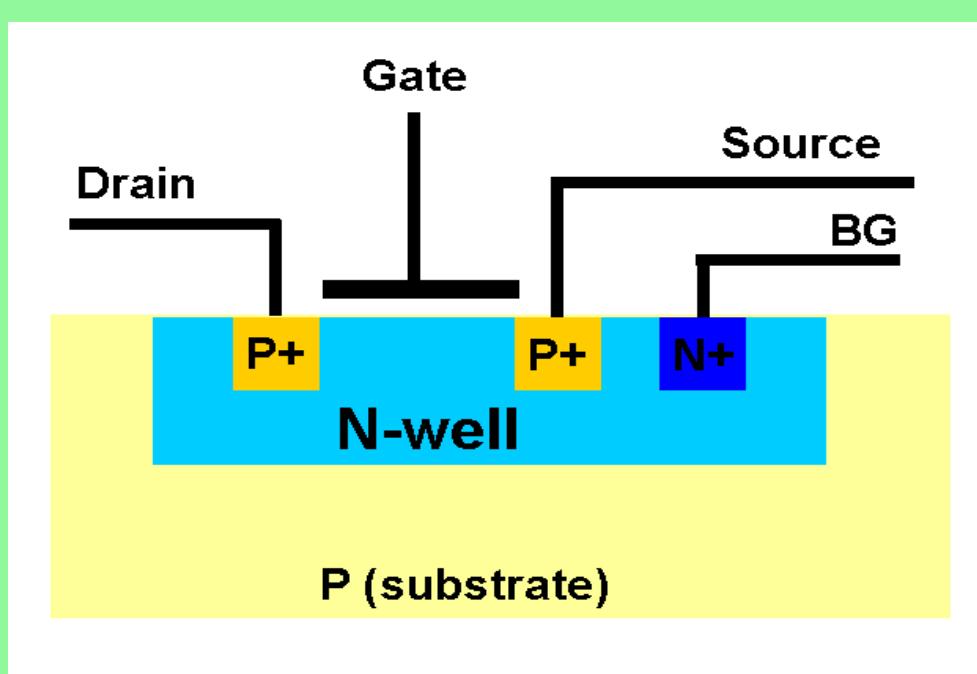
Toyoki Watabe, Takanori Hirao, Hiroshi Shibai, Mitsunobu Kawada,  
Hirohisa Nagata, Yasunori Hibi Nagoya University  
Manabu Noda Nagoya City Science Museum  
Takao Nakagawa

The Institute of Space and Astronautical Science

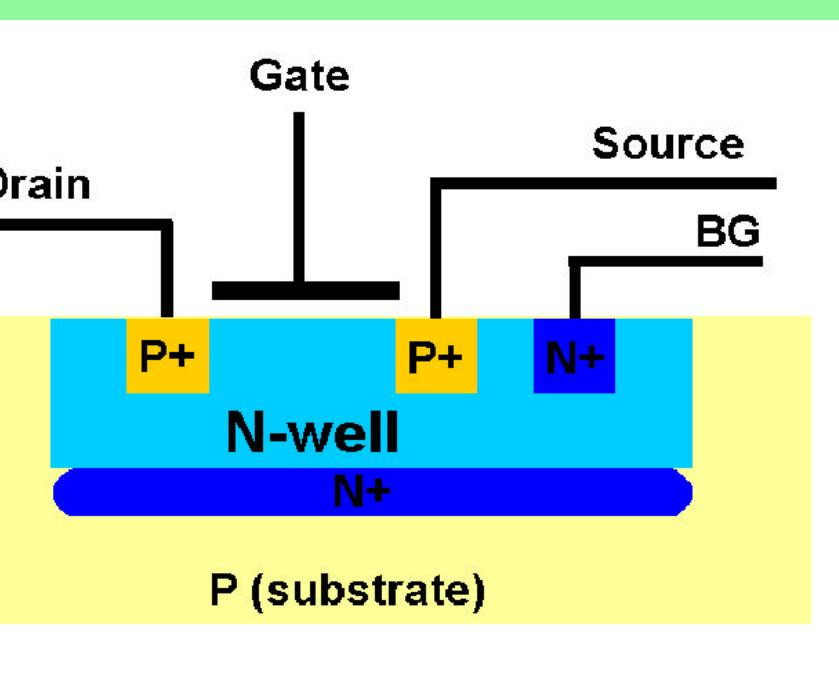


## CMOS Structure and Characteristics at 4.2K

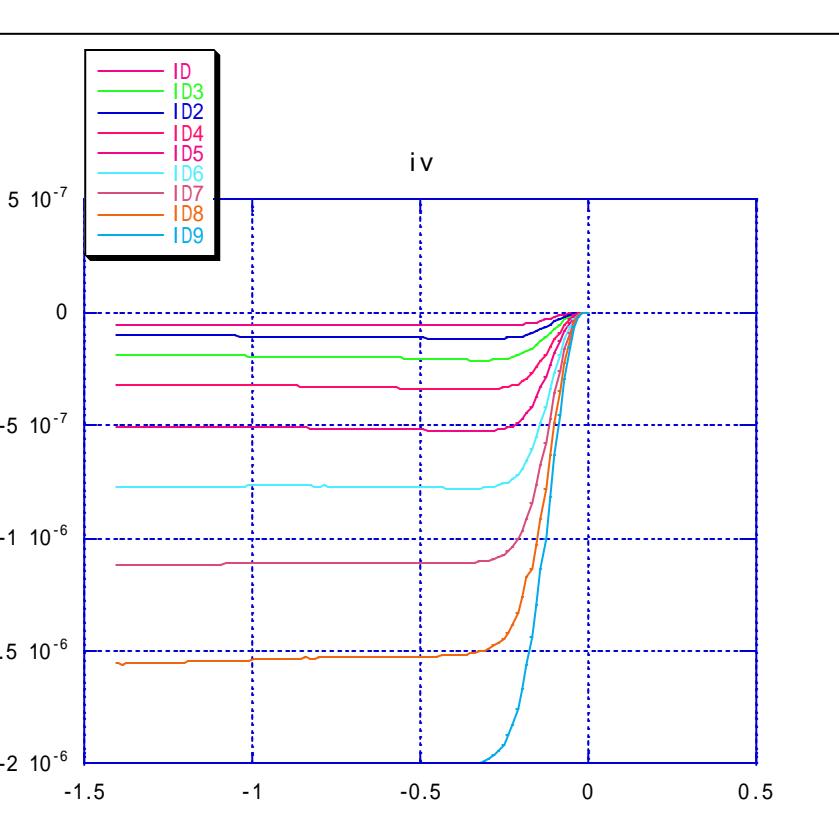
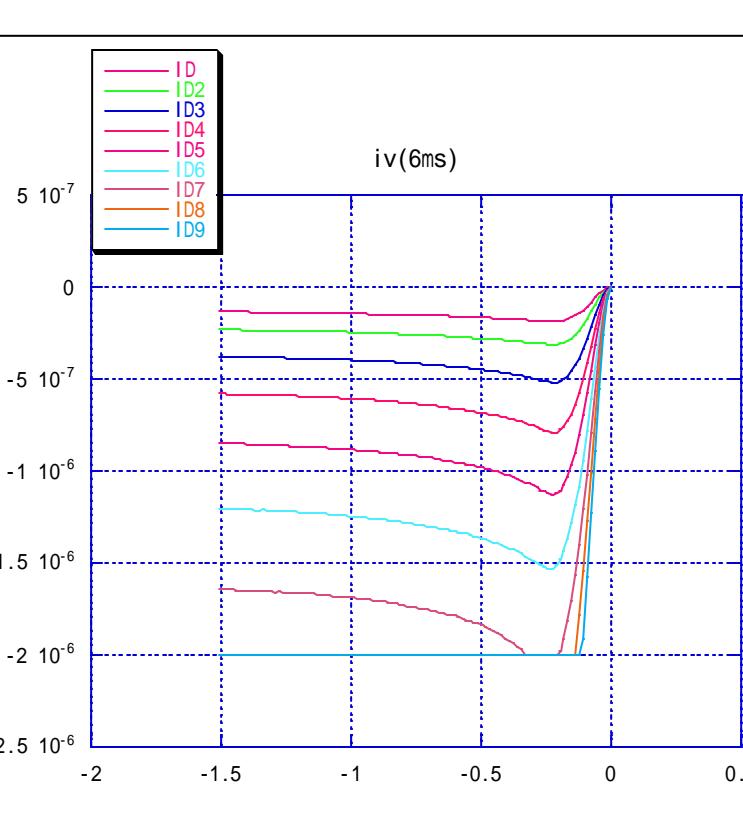
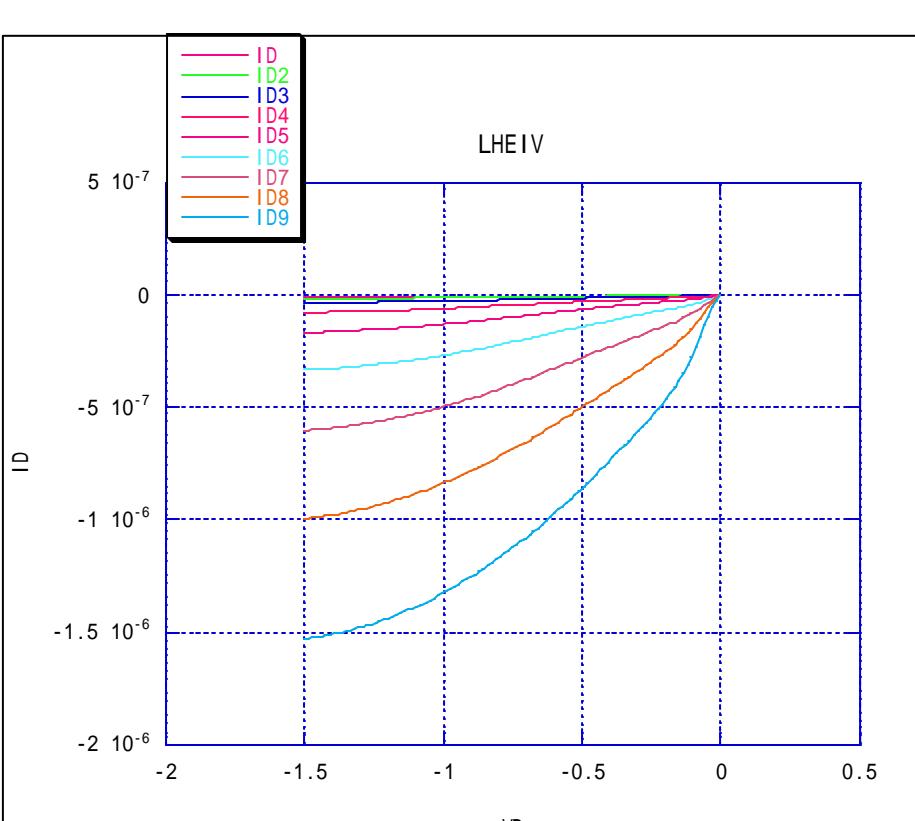
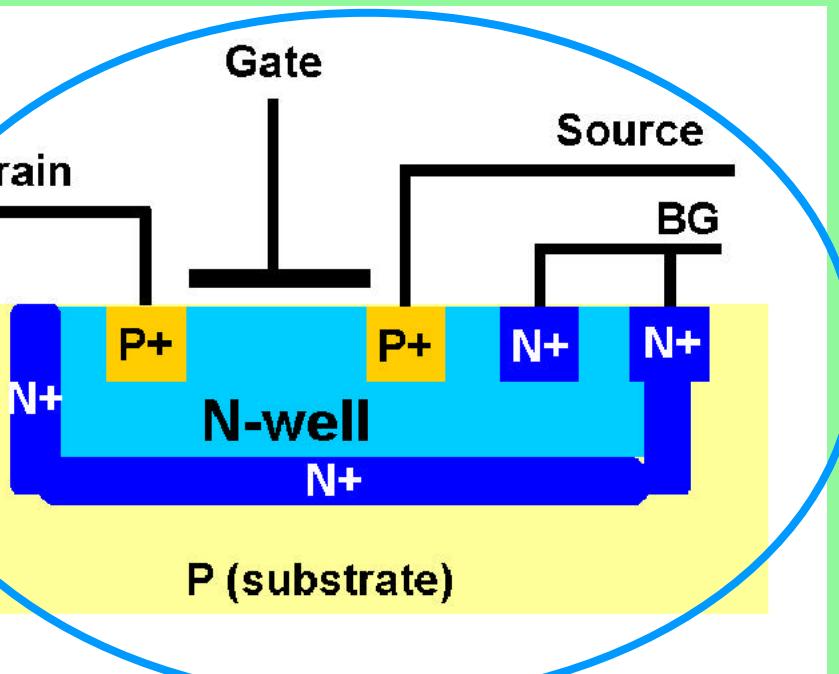
Standard CMOS process



Bi-CMOS process



Bi-CMOS process  
and Ion dope



This amplifier was made of 3-stage differential amp, dc offset cancel and source follower buffer for output.

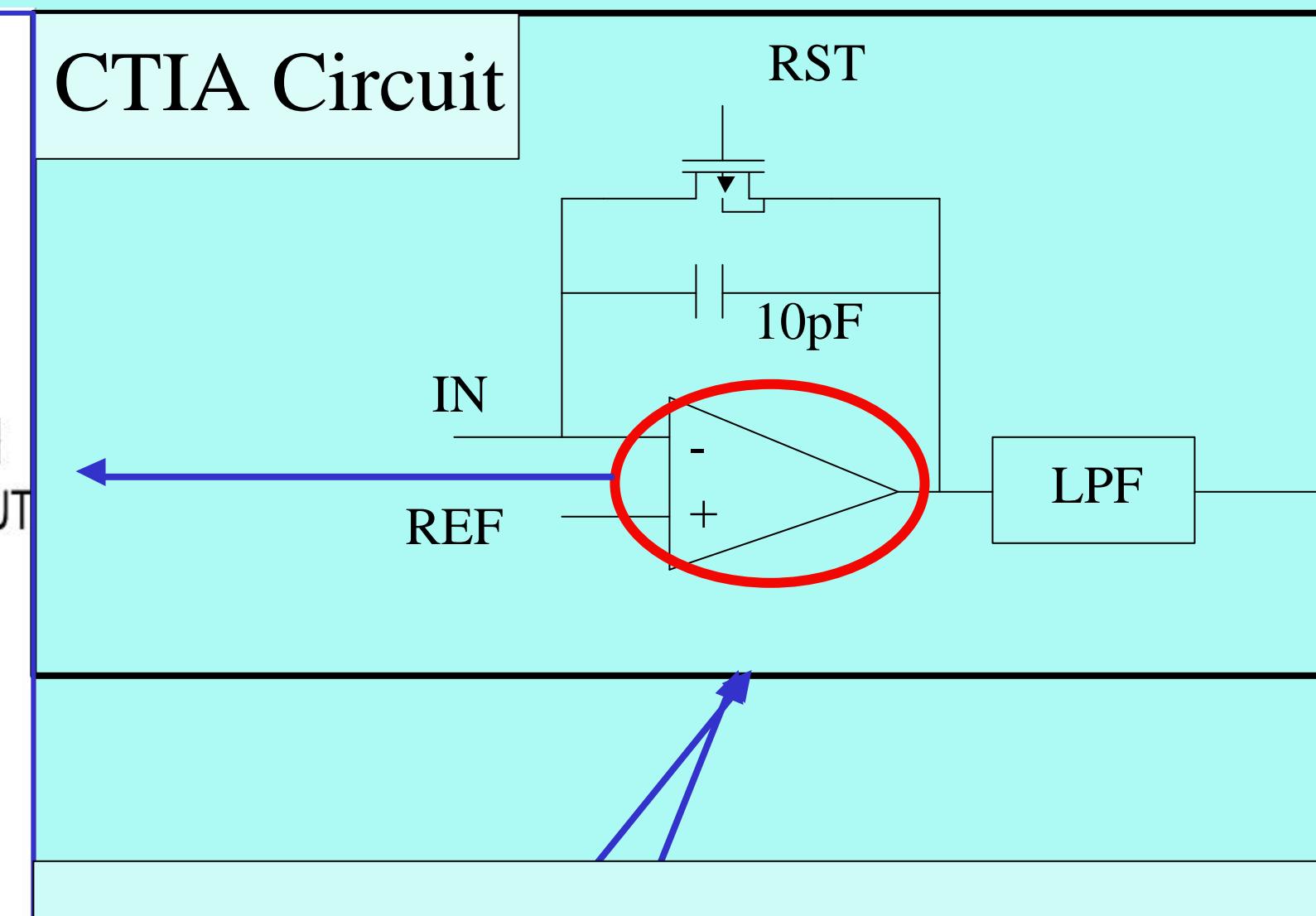
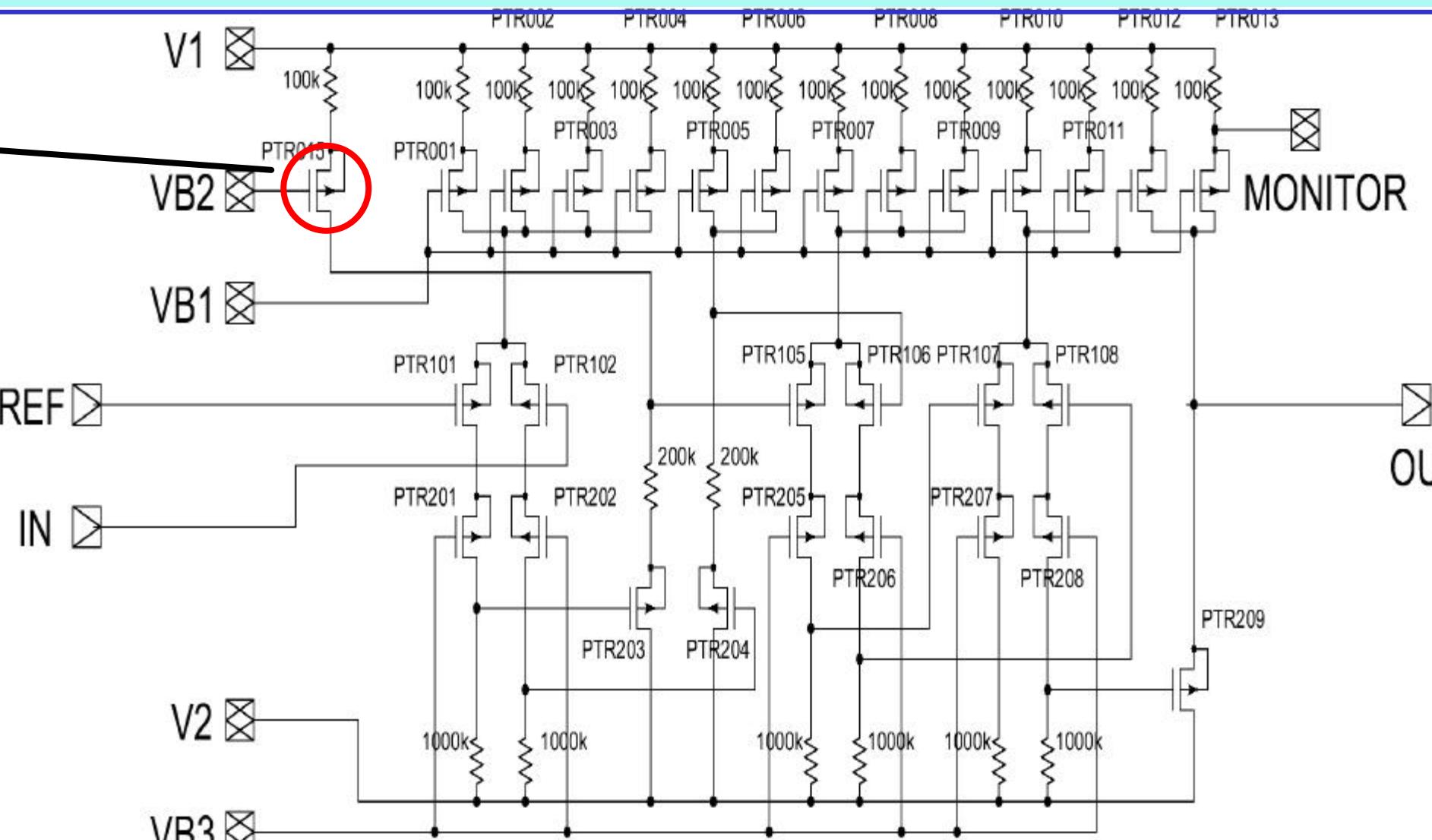
V1 and V2 are for power line.

VB1 is the bias voltage of constant current control.

VB2 is bias voltage for dc offset control .

IN is inverting input of the differential amplifier and REF is non-inverting input.

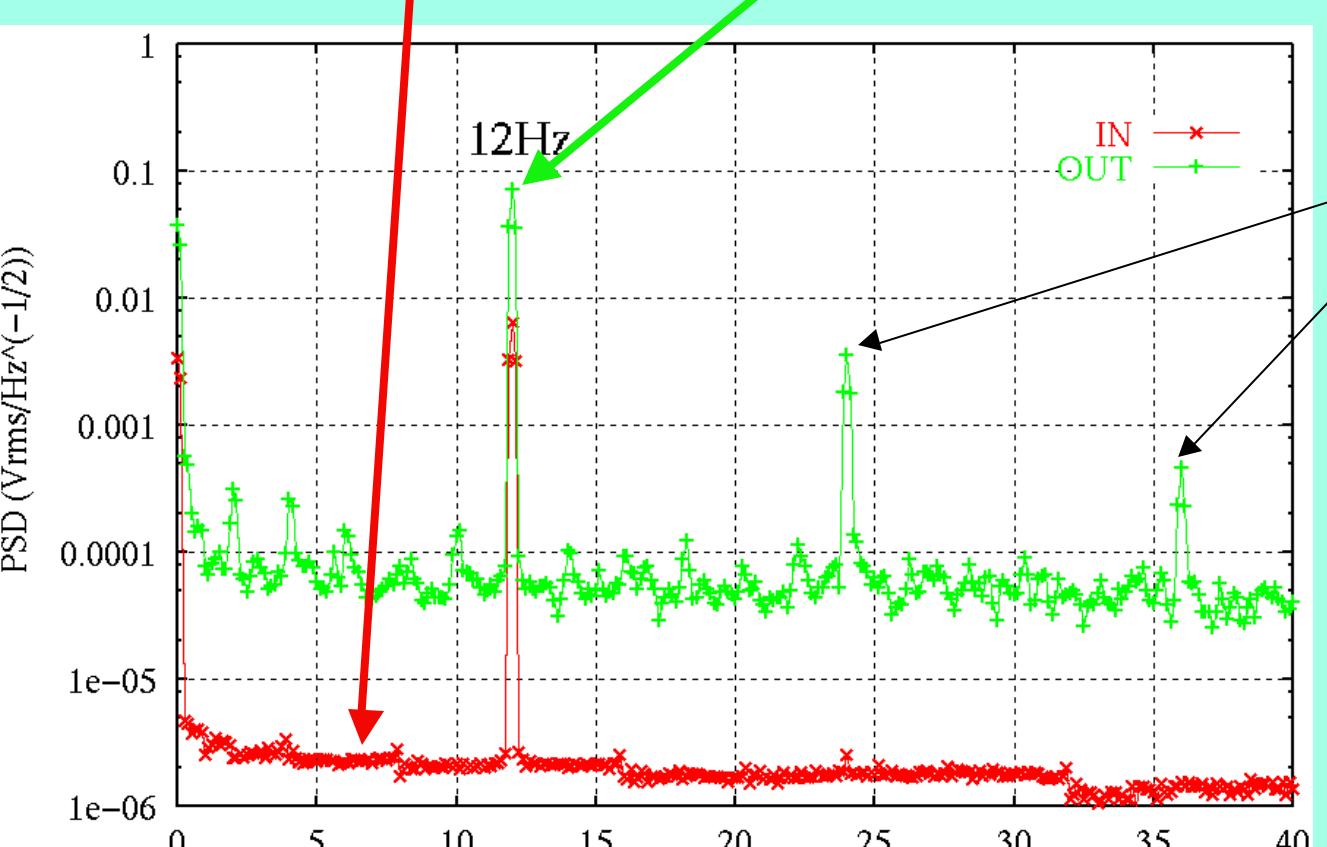
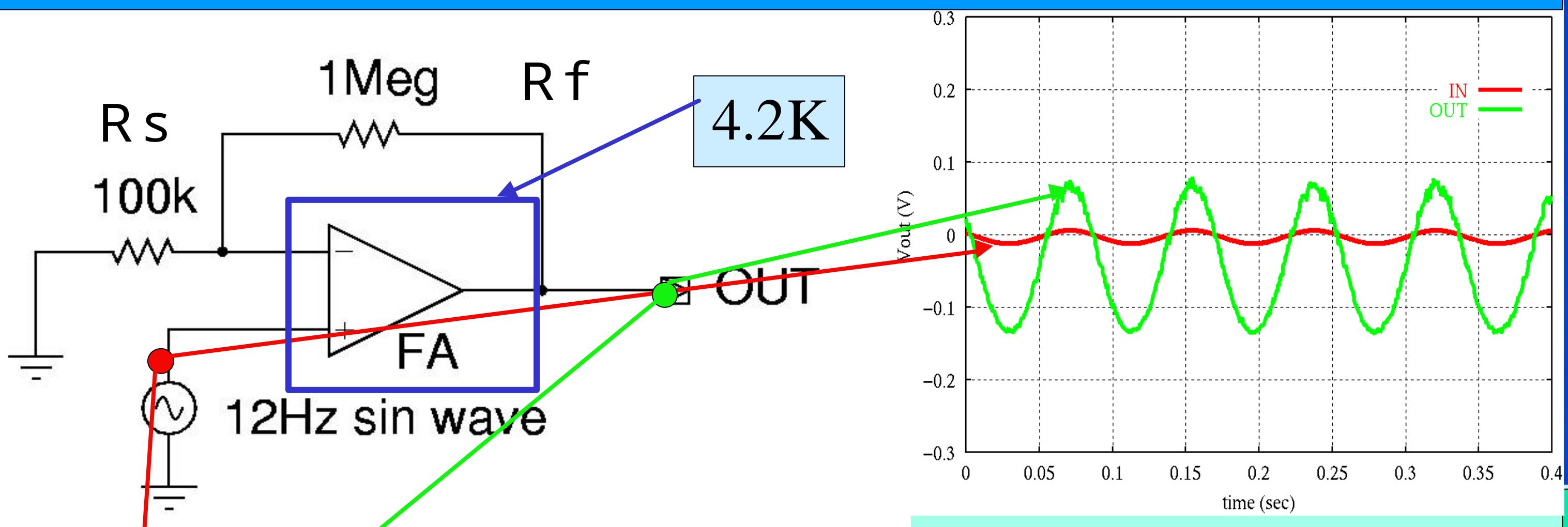
VB3 is cascade amplifier control line.



CIRCUIT DIAGRAM of FA-AMP(Differential Amplifier)

FA 5 have 5channel CTIA circuits on the chip.  
FA 60 have 60 channel CTIA circuits.

## Differential-Amplifier Test circuit and result



$$\text{Open loop gain is calculated} = R_s(R_s + R_f)$$

$$A = V_o / (V_o - V_s)$$

Distortion

Operating parameters at 4.2K  
V1 = +1.8V  
V2 = -1.8V  
VB1 = +0.306V  
VB2 = +0.402V  
VB3 = -2.9V

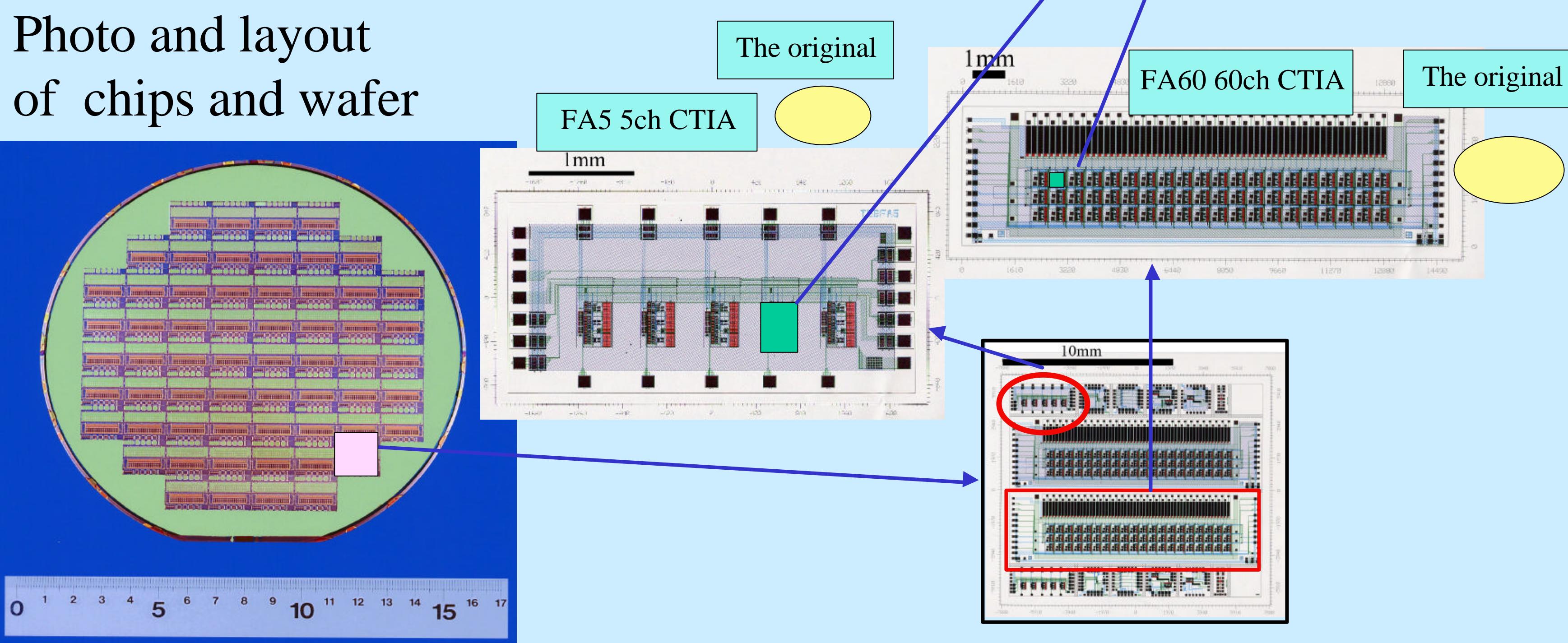
$$A \sim 300$$

$$P_o = 9.6 \mu W$$

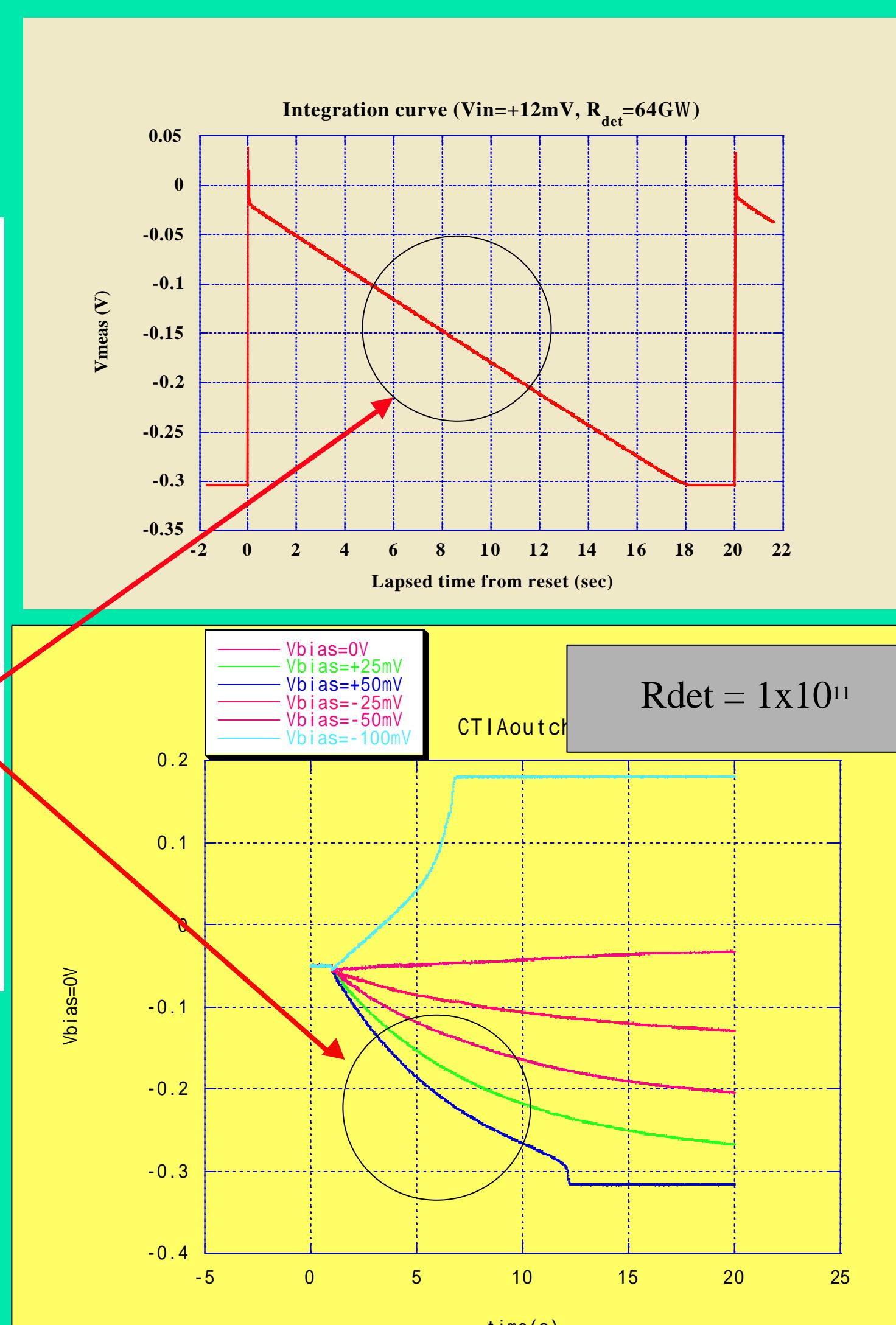
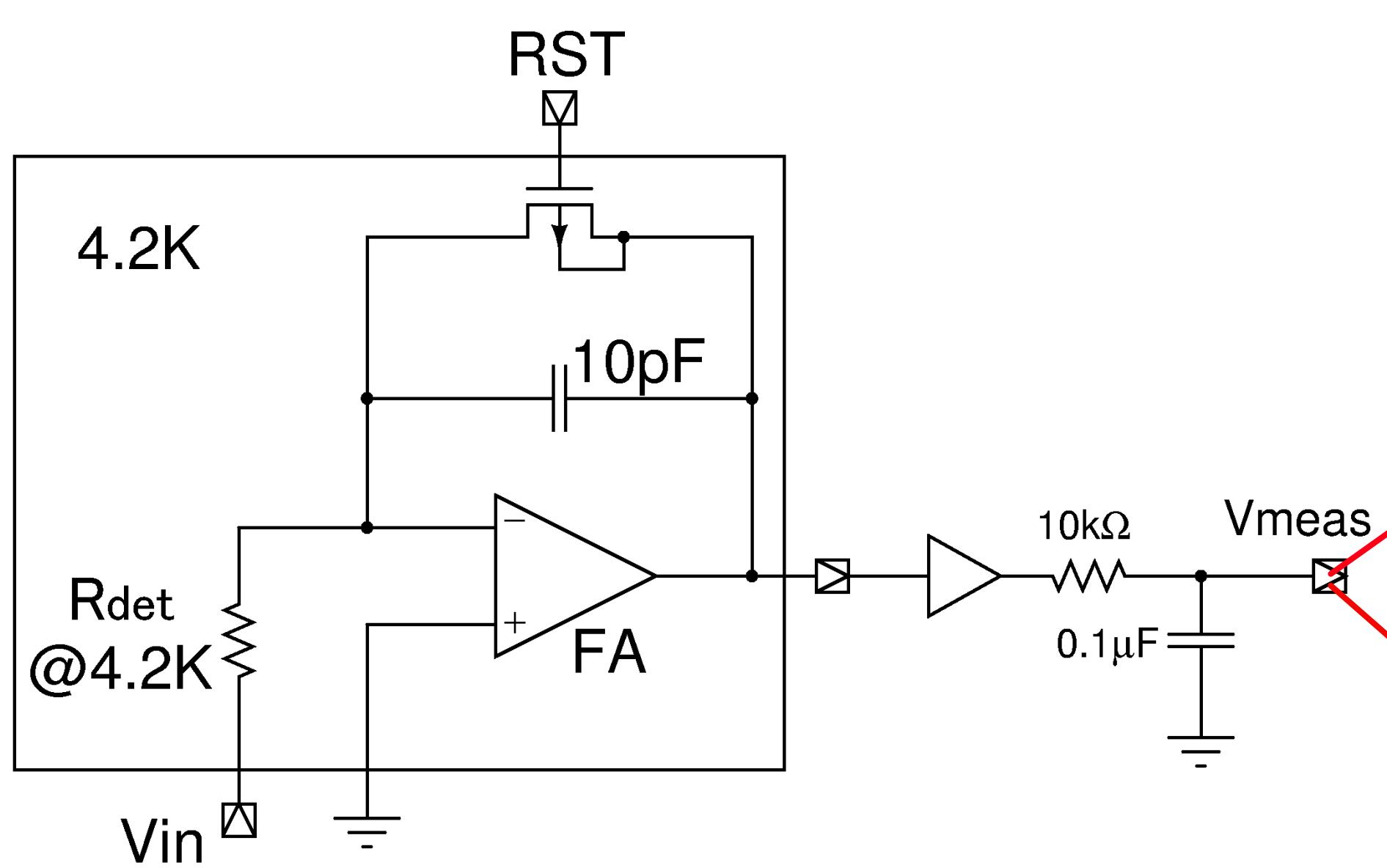
## Result

Success to develop the CRE  
Differential amp gain ~ 300  
Power consumption less than 10  $\mu$  W  
Need more TEST

## Photo and layout of chips and wafer



## CTIA Test circuit and results at the 4.2K



## Result

CTIA circuit was working at 4.2K  
Power consumption less than 10  $\mu$  W

Need more Test to tune the voltage and bias (VB1,VB2) parameter at 4.2K